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EXAMINER
TSAI, SHENG JEN

ART UNIT	PAPER NUMBER
2186	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/707,138	CHOU ET AL.	
	Examiner	Art Unit	
	Sheng-Jen Tsai	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/22/03, 12/29/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-20 are presented for examination in this application (10,707,138) filed on November 22, 2003.

Acknowledgement is made to the Information Disclosure Statement received on 11/22/2003 and 12/29/2003.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 1-20 are rejected under the judicially created doctrine of anticipation-type double patenting as being anticipated by claims 1-20 of US patent **6,874,044** (Chou et al., "Flush Drive/Reader with Serial-Port Controller and Flash-Memory Controller Mastering a Second RAM-Buffer Bus Parallel to a CPU Bus"), as shown in the following table. Although not all of the conflicting claims are exactly identical, they are extremely similar and are not patentably distinct from each other as explained in the "explanation" column of the table below:

6,874,044	**10/707,138**
1. A flash-memory peripheral comprising: a local central processing unit (CPU) for executing instructions for operating the flash-memory peripheral; a CPU bus primarily controlled by the local CPU; a flash-serial buffer bus not primarily controlled by the local CPU; a RAM buffer for storing flash data for storage by the flash-memory peripheral; a flash-memory controller for controlling a flash memory that stores the flash data, having a slave port for coupling to the CPU bus and receiving commands from the local CPU, and having a master port for coupling to the flash-serial buffer bus for transferring flash data to the RAM buffer; a serial link for connecting the flash-memory peripheral to a personal computer; and a serial engine for sending and receiving the flash data serially over the serial link, the serial engine having a slave port for coupling to the CPU bus and receiving commands from the local CPU, and having a master port for coupling to the flash-serial buffer bus for transferring flash data to the RAM buffer; wherein the flash data is read from the flash memory by the flash-memory controller and sent over the flash-serial buffer bus to the RAM buffer; wherein the flash data is read from the RAM buffer through the flash-serial buffer bus to the serial engine to be sent serially over the serial link, wherein incoming flash data is written to the RAM buffer through the flash-serial buffer bus from the serial engine, wherein the incoming flash data is read from the RAM buffer through the flash-serial buffer bus to the flash-memory controller and written to the flash memory, whereby the flash-serial buffer bus transfers the flash data and the CPU bus sends commands to the flash-memory controller and to the serial engine.	1. An ExpressCard comprising: an ExpressCard connector for mating with a host ExpressCard connector on a host; a first flash-memory chip for storing data; a second flash-memory chip for storing data; a controller chip, coupled to the ExpressCard connector, for controlling communication to the host through the ExpressCard connector; a first flash-memory channel between the controller chip and the first flash-memory chip, the first flash-memory channel having a first data bus for communicating data between the controller chip and the first flash-memory chip; a second flash-memory channel between the controller chip and the second flash-memory chip, the second flash-memory channel having a second data bus for communicating data between the controller chip and the second flash-memory chip; a shared control bus between the controller chip and the first and second flash-memory chips; a first response line from the first flash-memory chip to the controller chip for indicating completion of an operation by the first flash-memory chip; and a second response line from the second flash-memory chip to the controller chip for indicating completion of an operation by the second flash-memory chip, whereby the ExpressCard has two channels to the first and second flash-memory chips but a shared control bus to the first and second flash-memory chips.

2. The flash-memory peripheral of claim 1 further comprising: a first slave port on the RAM buffer, for connecting the CPU bus to the RAM buffer; a second slave port on the RAM buffer, for connecting the flash-serial buffer bus to the RAM buffer, whereby the RAM buffer has two slave ports to connect to two buses.	2. The ExpressCard of claim 1 further comprising: a housing for enclosing the controller chip and the first and second flash-memory chips; wherein the housing has an opening on an insertion end for the ExpressCard connector.
3. The flash-memory peripheral of claim 2 further comprising: a read-only-memory ROM, coupled to the local CPU, for storing instructions to be executed by the local CPU including instructions to send commands to the flash-memory controller or to the serial engine.	3. The ExpressCard of claim 2 wherein the housing contains a cutout notch wherein a first width of the insertion end containing the ExpressCard connector is narrower than a second width of an opposite end that is opposite the insertion end.
4. The flash-memory peripheral of claim 3 wherein the ROM is coupled to the local CPU through the CPU bus or through a ROM bus separate from the CPU bus.	4. The ExpressCard of claim 2 wherein the first response line carries a ready signal from the first flash-memory chip; wherein the second response line carries a ready signal from the second flash-memory chip, whereby separate ready signals are sent to the controller chip.
5. The flash-memory peripheral of claim 2 further comprising: a flash memory for storing the flash data, the flash memory permanently connected to the flash-memory controller, wherein the flash-memory peripheral is a flash drive.	5. The ExpressCard of claim 4 wherein the controller chip further comprises: a serial engine, coupled to the ExpressCard connector, for sending and receiving serial signals representing data and commands from the host; a flash-memory controller for generating control signals on the shared control bus to the first and second flash-memory chips; a central processing unit (CPU) for executing routines of instructions to transfer data between the serial engine and the flash-memory controller.
6. The flash-memory peripheral of claim 2 further comprising: a slot for accepting a flash-memory card removably inserted by a user; wherein the flash-memory controller is a flash-card controller connected to the slot; wherein the flash-memory peripheral is a flash-card reader.	6. The ExpressCard of claim 5 wherein the controller chip further comprises an internal bus between the CPU, the serial engine, and the flash-memory controller.
7. The flash-memory peripheral of claim 2 further comprising: a plurality of slots each for accepting a flash-memory card for storing the flash data; a plurality of flash-card controllers, coupled to the plurality of slots to read flash-memory cards inserted into the plurality of slots, each flash-card controller having a slave port coupled to the CPU bus to receive commands from the local CPU, and each having a master port coupled to the flash-serial buffer bus, for transferring flash data to the RAM buffer, wherein the flash-memory peripheral is a multi-slot flash-card reader.	7. The ExpressCard of claim 5 wherein the controller chip further comprises: a system buffer for temporarily storing data transferred between the serial engine and the flash-memory controller; a scratch-pad random-access memory (RAM) for storing parameters used by the CPU; and a read-only memory (ROM) for storing the routines of instructions executed by the CPU.
8. The flash-memory peripheral of claim 2 wherein	8. The ExpressCard of claim 5 wherein the controller chip

the serial link is a Universal-Serial-Bus (USB).	further comprises: an error-correction code (ECC) generator, coupled to the flash-memory controller, for appending ECC bits to data being written to the first or second flash-memory chips, and for reading ECC bits and correcting errors in data read from the first or second flash-memory chips, whereby data errors are corrected by error-correction code.
9. The flash-memory peripheral of claim 2 wherein the serial link is a IEEE 1394 bus, an Integrated-Device-Electronics (IDE) bus, a serial AT-attachment (SATA) bus, a PCI Express bus, or a mini-PCI Express bus.	9. The ExpressCard of claim 5 wherein the routines of instructions include routines to erase, read, or write data in the first or second flash-memory chips.
10. A flash reader comprising: a local processor that executed instructions for controlling operation of the flash reader; a processor bus, mastered by the local processor, for sending commands from the local processor; a buffer bus, not connected to the local processor, for transferring flash data; a RAM buffer for storing flash data; a flash-memory controller for reading flash data from a flash memory in response to commands from the local processor; a serial engine for sending the flash data as serial data over a serial interface; a flash slave port, on the flash-memory controller, for connecting the flash-memory controller to the processor bus as a bus-slave device; a flash master port, on the flash-memory controller, for connecting the flash-memory controller to the buffer bus when the flash-memory controller acts as a bus-master device; an engine slave port, on the serial engine, for connecting the serial engine to the processor bus as a bus-slave device; an engine master port, on the serial engine, for connecting the serial engine to the buffer bus when the serial engine acts as the bus-master device; a first slave port, on the RAM buffer, for connecting the RAM buffer to the processor bus as a bus-slave device; and a second slave port, on the RAM buffer, for connecting the RAM buffer to the buffer bus as a bus-slave device when the flash-memory controller or the serial engine acts as the bus-master device, whereby the processor bus transfers commands while the buffer bus transfers the flash data bypassing the local processor.	10. The ExpressCard of claim 9 wherein the controller chip further comprises: an input-output interface for driving an indicator lamp when the flash-memory controller is reading or writing to the first or second flash-memory chips.
11. The flash reader of claim 10 wherein the processor bus acts independently of the buffer bus, the local processor able to send commands over the processor bus independent of and at a same time as flash data is transferred over the buffer bus.	11. The ExpressCard of claim 5 wherein the shared control bus comprises a read-enable signal and a write-enable signal that are connected to both the first and second flash-memory chips.
12. The flash reader of claim 11 wherein the local processor reads flash data from the RAM buffer, modifies the flash data, and writes modified flash	12. The ExpressCard of claim 11 wherein the shared control bus further comprises: a command latch enable signal to latch a command into the first or second flash-

data back to the RAM buffer, using the processor bus and the first slave port of the RAM buffer, whereby the local processor can modify the flash data stored in the RAM buffer using the processor bus.	memory chips; an address latch enable signal to latch an address into the first or second flash-memory chips.
13. The flash reader of claim 11 wherein the flash-memory controller is a first flash-card controller connected to a first slot for receiving a first flash-memory card that stores flash data; further comprising: a second flash-card controller connected to a second slot for receiving a second flash-memory card that stores flash data; a second flash slave port, on the second flash-card controller, for connecting the second flash-card controller to the processor bus as a bus-slave device; a second flash master port, on the second flash-card controller, for connecting the second flash-card controller to the buffer bus when the second flash-card controller acts as a bus master device, whereby multiple flash-cards can be read by flash reader.	13. The ExpressCard of claim 12 wherein the shared control bus comprises a shared chip-select signal to enable the first flash-memory chip and the second flash-memory chip.
14. The flash reader of claim 11 wherein the RAM buffer stores pre-fetched blocks of the flash data read by the flash-memory controller into the RAM buffer before the serial engine requests the pre-fetched blocks, whereby pre-fetched flash data is stored by the RAM buffer.	14. The ExpressCard of claim 5 wherein the ExpressCard connector has a pair of differential data lines for communicating data and commands from the host to the controller chip.
15. The flash reader of claim 11 wherein the RAM buffer comprises: a write buffer storing flash data from the serial engine for writing to the flash memory by the flash-memory controller; a read buffer storing flash data from the flash memory written to the RAM buffer by the flash-memory controller.	15. The ExpressCard of claim 14 wherein the pair of differential data lines comprise Universal-Serial-Bus (USB) data lines, wherein the controller chip is a USB slave and the host is a USB host.
16. The flash reader of claim 15 wherein the write buffer and the read buffer are FIFO buffer regions in the RAM buffer.	16. A flash-storage ExpressCard comprising: connector means for connecting to a host; controller means for performing control functions; flash-memory means for storing data in non-volatile memory; a first channel between the controller means and the flash-memory means, the first channel having a first data bus and a first ready means for indicating when a first flash-memory chip in the flash-memory means is busy; a second channel between the controller means and the flash-memory means, the second channel having a second data bus and a second ready means for indicating when a second flash-memory chip in the flash-memory means is busy; shared control bus means for sending flash control signals to flash-memory means; flash-control means, in the controller means, for generating the flash control signals to the shared control bus means; and serial control means, in the controller means, for serially communicating with the host through the connector means.
17. The flash reader of claim 11 further comprising:	17. The flash-storage ExpressCard of claim 16 wherein

interface logic, coupled to the processor bus and coupled to the buffer bus, for connecting the processor bus or the buffer bus to an external RAM buffer for storing an overflow of flash data, whereby overflow flash data is stored in the external RAM buffer.	the serial control means comprises a Universal-Serial-Bus (USB) controller, and wherein the connector means includes a differential pair of serial data lines that carry serial USB signals between the host and the controller means, or wherein the serial control means comprises a Peripheral Component Interconnect (PCI) Express controller, and wherein the connector means includes a differential pair of PCI-Express-transmit serial data lines and a differential pair of PCI-Express-receive serial data lines that carry serial signals between the host and the controller means.
18. A flash device comprising: processor means for executing controlling instructions; first bus means for transferring commands from the processor means; buffer bus means for transferring flash data that by-passes the processor means; data buffer means, coupled to the buffer bus means as a bus slave, for storing flash data being read by the flash device; flash-memory controller means, coupled to the first bus means as a bus slave, and coupled to the buffer bus means as a bus master, for controlling a flash memory and for reading flash data from the flash memory; and serial engine means, coupled to the first bus means as a bus slave, and coupled to the buffer bus means as a bus master, for reading flash data stored by the data buffer means and for serially transmitting the flash data over a serial link; wherein the flash data is transferred from the flash-memory controller means to the data buffer means over the buffer bus means bypassing the processor means; wherein the flash data is transferred from the data buffer means to the serial engine means over the buffer bus means bypassing the processor means, whereby transfers of the flash data use the buffer bus means to bypass the processor means.	18. The flash-storage ExpressCard of claim 16 wherein the serial control means comprises both a Universal-Serial-Bus (USB) controller, and a Peripheral Component Interconnect (PCI) Express controller; and wherein the connector means includes a differential pair of serial data lines that carry serial USB signals between the host and the controller means when using the USB controller, and a differential pair of PCI-Express-transmit serial data lines and a differential pair of PCI-Express-receive serial data lines that carry serial signals between the host and the controller means when using the PCI Express controller, whereby dual serial controllers allow communication with the host using either USB or PCI Express.
19. The flash device of claim 18 wherein the buffer bus means is unconnected to the processor means, but the data buffer means is connected to the first bus means as a bus slave; wherein the serial link is a Universal-Serial-Bus (USB), a IEEE 1394 bus, a PCI Express bus, or a mini-PCI Express bus.	19. An interleaved flash ExpressCard comprising: an ExpressCard connector for plugging into a host; a controller chip that has a microprocessor core, a program memory, a buffer memory, a serial controller, and a flash controller; a first flash-memory chip in a first channel; a second flash-memory chip in the first channel; a third flash-memory chip in the first channel; a fourth flash-memory chip in the first channel; a shared control bus having a write-enable signal, a read-enable signal, and latch-enable signals generated by the flash controller in the controller chip and driven to the first, second, third, and fourth flash-memory chips; a first data bus between the controller chip and the first and third flash-memory chip; a first shared ready signal generated by the first flash-memory chip and the second flash-memory chip and driven to the controller chip; a second data bus between the controller chip and the second and fourth flash-memory chip; and a second shared ready signal generated by the third flash-memory chip and the fourth flash-memory chip and driven to the controller chip; a first chip select generated by the controller chip and connected to the first and second flash-memory chip; a second chip select

	generated by the controller chip and connected to the third and fourth flash-memory chip; wherein the serial controller in the controller chip is a Universal-Serial-Bus (USB) controller that communicates to the host using a pair of differential USB data signals in the ExpressCard connector, or the serial controller in the controller chip is a Peripheral Component Interconnect (PCI) Express controller, a Firewire controller, a serial ATA controller, or a serial small-computer system interface (SCSI) controller; wherein access to the first and third flash-memory chips is interleaved; wherein access to the second and fourth flash-memory chips is interleaved.
20. The flash device of claim 19 wherein the serial link connects to a personal computer that has a static random-access memory (SRAM) buffer for storing blocks of data generated by a CPU on the personal computer for transfer over the serial link and storage as flash data by the flash device.	20. An interleaved dual-channel flash ExpressCard comprising: an ExpressCard connector for plugging into a host; a controller chip that has a microprocessor core, a program memory, a buffer memory, a serial controller, and a flash controller; a first flash-memory chip in a first channel; a second flash-memory chip in a second channel; a third flash-memory chip in the first channel; a fourth flash-memory chip in the second channel; a first shared control bus having a write-enable signal, a read-enable signal, and latch-enable signals generated by the flash controller in the controller chip and driven to the first and third flash-memory chips; a first data bus between the controller chip and the first and third flash-memory chip; a first ready signal generated by the first flash-memory chip and driven to the controller chip; a third ready signal generated by the third flash-memory chip and driven to the controller chip; a second shared control bus having a write-enable signal, a read-enable signal, and latch-enable signals generated by the flash controller in the controller chip and driven to the second and fourth flash-memory chips; a second data bus between the controller chip and the second and fourth flash-memory chip; and a second ready signal generated by the second flash-memory chip and driven to the controller chip; and a fourth ready signal generated by the fourth flash-memory chip and driven to the controller chip; wherein the serial controller in the controller chip is a Universal-Serial-Bus (USB) controller that communicates to the host using a pair of differential USB data signals in the ExpressCard connector, or the serial controller in the controller chip is a Peripheral Component Interconnect (PCI) Express controller, a Firewire controller, a serial ATA controller, or a serial small-computer system interface (SCSI) controller, wherein access to the first and third flash-memory chips is interleaved; wherein access to the second and fourth flash-memory chips is interleaved.

4. Claims 1-20 are rejected under the judicially created doctrine of anticipation-type double patenting as being anticipated by claims 1-20 of US patent **6,993,618** (Chen et al., "Dual-Mode Flash Storage Exchanger that Transfers Flash-Card Data to a

Removable USB Flash Key-Drive with or without a PC Host"), as shown in the following table. Although not all of the conflicting claims are exactly identical, they are extremely similar and are not patentably distinct from each other as explained in the "explanation" column of the table below:

6,993,618	**10/707,138**
1. A flash-card reader and exchanger comprising: a first serial-bus connector for receiving a serial cable connected to a host computer that acts as a serial-bus host; a second serial-bus connector for receiving a serial-bus flash-memory drive; a serial bus connected to the first and second serial-bus connectors; an input-output bus; a dual-mode microcontroller coupled to the serial bus and coupled to the input-output bus, for operating in a card-reader mode and responding as a serial-bus peripheral to requests from the host computer when the host computer is connected, but for operating in an exchanger mode and originating data transfers as a local host of the serial bus when the host computer is not connected to the first serial-bus connector; a flash-card interface for receiving a removable flash-memory card, the flash-card interface connected to the input-output bus; and an exchanger program, executed by the dual-mode microcontroller, for reading data from the removable flash-memory card over the input-output bus to the dual-mode microcontroller, and for writing data over the serial bus to the serial-bus flash-memory drive, when the dual-mode microcontroller is operating in the exchanger mode, whereby the flash-card reader and exchanger operates in the card-reader mode when the host computer is connected, but operates in the exchanger mode, originating data transfers as a local host, when the host computer is not connected.	1. An ExpressCard comprising: an ExpressCard connector for mating with a host ExpressCard connector on a host; a first flash-memory chip for storing data; a second flash-memory chip for storing data; a controller chip, coupled to the ExpressCard connector, for controlling communication to the host through the ExpressCard connector; a first flash-memory channel between the controller chip and the first flash-memory chip, the first flash-memory channel having a first data bus for communicating data between the controller chip and the first flash-memory chip; a second flash-memory channel between the controller chip and the second flash-memory chip, the second flash-memory channel having a second data bus for communicating data between the controller chip and the second flash-memory chip; a shared control bus between the controller chip and the first and second flash-memory chips; a first response line from the first flash-memory chip to the controller chip for indicating completion of an operation by the first flash-memory chip; and a second response line from the second flash-memory chip to the controller chip for indicating completion of an operation by the second flash-memory chip, whereby the ExpressCard has two channels to the first and second flash-memory chips but a shared control bus to the first and second flash-memory chips.
2. The flash-card reader and exchanger of claim 1 wherein the serial bus is a PCI Express bus, an Express-Card bus, a Firewire (IEEE 1394) bus, a serial ATA bus, or a serial attached small-computer system interface (SCSI) bus.	2. The ExpressCard of claim 1 further comprising: a housing for enclosing the controller chip and the first and second flash-memory chips; wherein the housing has an opening on an insertion end for the ExpressCard connector.
3. The flash-card reader and exchanger of claim 1 wherein the serial bus is a Universal-Serial-Bus (USB).	3. The ExpressCard of claim 2 wherein the housing contains a cutout notch wherein a first width of the insertion end containing the ExpressCard connector is narrower than a second width of an opposite end that is opposite the insertion end.
4. The flash-card reader and exchanger of claim 3 wherein the dual-mode microcontroller is a USB On-the-Go controller or a USB reduced-function host	4. The ExpressCard of claim 2 wherein the first response line carries a ready signal from the first flash-memory chip; wherein the second response line carries a ready signal

controller acting as a USB host when not connected to the host computer, but acting as a USB peripheral when connected to the host computer.	from the second flash-memory chip, whereby separate ready signals are sent to the controller chip.
5. The flash-card reader and exchanger of claim 3 wherein the dual-mode microcontroller comprises: a serial interface to a serial bus that connects to a host; a serial engine for detecting and processing packets sent over the serial bus; a serial-engine buffer for storing data sent over the serial bus; an internal bus coupled to the serial-engine buffer; a random-access memory (RAM) for storing instructions for execution, the RAM on the internal bus; a central processing unit, on the internal bus, the CPU accessing and executing instructions in the RAM; and an input-output controller, on the internal bus, for communicating with the input-output bus.	5. The ExpressCard of claim 4 wherein the controller chip further comprises: a serial engine, coupled to the ExpressCard connector, for sending and receiving serial signals representing data and commands from the host; a flash-memory controller for generating control signals on the shared control bus to the first and second flash-memory chips; a central processing unit (CPU) for executing routines of instructions to transfer data between the serial engine and the flash-memory controller.
6. The flash-card reader and exchanger of claim 5 further comprising: an indicator lamp for indicating when data is being transferred by the dual-mode microcontroller; and a user-activated button for initiating data transfer, wherein the indicator lamp and the user-activated button are connected to the input-output bus.	6. The ExpressCard of claim 5 wherein the controller chip further comprises an internal bus between the CPU, the serial engine, and the flash-memory controller.
7. The flash-card reader and exchanger of claim 6 wherein the indicator lamp comprises: a first direction lamp that indicates when the removable flash-memory card is to be read; a second direction lamp that indicates when the removable flash-memory card is to be written; a card-reader mode lamp that indicates when the dual-mode microcontroller is operating in the card-reader mode; and an exchanger mode lamp that indicates when the dual-mode microcontroller is operating in the exchanger mode.	7. The ExpressCard of claim 5 wherein the controller chip further comprises: a system buffer for temporarily storing data transferred between the serial engine and the flash-memory controller; a scratch-pad random-access memory (RAM) for storing parameters used by the CPU; and a read-only memory (ROM) for storing the routines of instructions executed by the CPU.
8. The flash-card reader and exchanger of claim 7 wherein the indicator lamp comprises at least one multi-color light-emitting diode (LED).	8. The ExpressCard of claim 5 wherein the controller chip further comprises: an error-correction code (ECC) generator, coupled to the flash-memory controller, for appending ECC bits to data being written to the first or second flash-memory chips, and for reading ECC bits and correcting errors in data read from the first or second flash-memory chips, whereby data errors are corrected by error-correction code.
9. The flash-card reader and exchanger of claim 7 further comprising: a card insertion lamp that indicates when the removable flash-memory card has been properly inserted into the flash-card interface.	9. The ExpressCard of claim 5 wherein the routines of instructions include routines to erase, read, or write data in the first or second flash-memory chips.
10. The flash-card reader and exchanger of claim 6 wherein the removable flash-memory card is a compact-flash card, a smart-media flash-card, a secure-digital/multi-media card, or a memory stick.	10. The ExpressCard of claim 9 wherein the controller chip further comprises: an input-output interface for driving an indicator lamp when the flash-memory controller is reading or writing to the first or second flash-memory chips.

11. The flash-card reader and exchanger of claim 10 further comprising: a flash-integrated memory module, coupled to the input-output bus; and a liquid crystal display (LCD), coupled to the input-output bus.	11. The ExpressCard of claim 5 wherein the shared control bus comprises a read-enable signal and a write-enable signal that are connected to both the first and second flash-memory chips.
12. The flash-card reader and exchanger of claim 6 wherein the exchanger program further comprises: a main control program that waits for insertion of the removable flash-memory card and activates the exchanger mode when the host computer is not connected to the serial bus, but activates the card-reader mode when the host computer is not connected to the serial bus.	12. The ExpressCard of claim 11 wherein the shared control bus further comprises: a command latch enable signal to latch a command into the first or second flash-memory chips; an address latch enable signal to latch an address into the first or second flash-memory chips.
13. The flash-card reader and exchanger of claim 12 further comprising: a flash-exchanger program, activated by the main control program when operating in the exchanger mode, the flash-exchanger program causing the dual-mode microcontroller to read data from the removable flash-memory card over the input-output bus, the flash-exchanger program causing the dual-mode microcontroller to send data to the serial-bus flash-memory drive as serial-bus packets; wherein the flash-exchanger program means includes means for reading a disk format of data, the disk format being File-Allocation Table (FAT), FAT32, New Technology File System (NTFS), Second Extended File System (Ext2), Third Extended File System (Ext3), Hierarchical File System (HFS), and Universal File System (UFS).	13. The ExpressCard of claim 12 wherein the shared control bus comprises a shared chip-select signal to enable the first flash-memory chip and the second flash-memory chip.
14. A user-expandable flash-card exchanger comprising: a local Universal-Serial-Bus (USB) segment; a host USB connector for connecting the local USB segment to a host computer that executes a USB host program to originate USB transfers; a second USB connector for receiving a USB-memory key drive, the USB-memory key drive having a flash memory for storing data from USB packets sent over the local USB segment; a USB dual-mode microcontroller, having a serial engine connected to the local USB segment, for executing a USB peripheral-mode program to respond to USB requests from the host computer during a peripheral mode, and for executing a local-host program to initiate data transfers when the host computer is not connected; an input-output bus, driven by the USB dual-mode microcontroller, for transferring data, addresses, and commands; a flash-card connector, coupled to the input-output bus, for receiving a removable flash-memory card; wherein the USB dual-mode microcontroller reads data from the removable flash-memory card over the input-output bus by sending flash-memory commands to the removable flash-memory card; an indicator on the input-output bus, for indicating operating status to a	14. The ExpressCard of claim 5 wherein the ExpressCard connector has a pair of differential data lines for communicating data and commands from the host to the controller chip.

user; and a user-input device on the input-output bus, for receiving an input from the user, whereby the USB dual-mode microcontroller operates as a USB peripheral when the host computer is attached, but executes the local-host program when the host computer is not connected.	
15. The user-expandable flash-card exchanger of claim 14 wherein the removable flash-memory card is a compact-flash card, a smart-media flash-card, a secure-digital/multi-media card, or a memory stick.	15. The ExpressCard of claim 14 wherein the pair of differential data lines comprise Universal-Serial-Bus (USB) data lines, wherein the controller chip is a USB slave and the host is a USB host.
16. The user-expandable flash-card exchanger of claim 15 further comprising: a second flash-card connector, for receiving a second type of removable flash-memory card that is a different type of removable flash-memory card that received by the flash-card connector, whereby at least two different types of the removable flash-memory card can be read.	16. A flash-storage ExpressCard comprising: connector means for connecting to a host; controller means for performing control functions; flash-memory means for storing data in non-volatile memory; a first channel between the controller means and the flash-memory means, the first channel having a first data bus and a first ready means for indicating when a first flash-memory chip in the flash-memory means is busy; a second channel between the controller means and the flash-memory means, the second channel having a second data bus and a second ready means for indicating when a second flash-memory chip in the flash-memory means is busy; shared control bus means for sending flash control signals to flash-memory means; flash-control means, in the controller means, for generating the flash control signals to the shared control bus means; and serial control means, in the controller means, for serially communicating with the host through the connector means.
17. The user-expandable flash-card exchanger of claim 14 wherein the USB dual-mode microcontroller comprises: an internal bus; a central processing unit, coupled to the internal bus, for executing instructions; a local program memory for storing program code executed by the central processing unit including the USB peripheral-mode program and the local-host program; an input-output controller, coupled to the internal bus and to the input-output bus; and wherein the serial engine comprises a serial interface to the local USB segment, and a serial-engine buffer, coupled to the internal bus, for storing data sent over the local USB segment.	17. The flash-storage ExpressCard of claim 16 wherein the serial control means comprises a Universal-Serial-Bus (USB) controller, and wherein the connector means includes a differential pair of serial data lines that carry serial USB signals between the host and the controller means, or wherein the serial control means comprises a Peripheral Component Interconnect (PCI) Express controller, and wherein the connector means includes a differential pair of PCI-Express-transmit serial data lines and a differential pair of PCI-Express-receive serial data lines that carry serial signals between the host and the controller means.
18. A flash-card exchanger comprising: dual-mode microcontroller means for executing control programs; a Universal-Serial-Bus (USB) connected to the dual-mode microcontroller means; first connector means, coupled to the USB, for receiving a USB-memory key drive that stores data contained in USB packets in response to USB requests; second connector means, coupled to the USB, for connecting to an external USB host that originates USB requests to the dual-mode microcontroller means; input-output bus means, controlled by the dual-mode microcontroller means; first flash interface means, connected to the input-output bus means, for interfacing to a removable flash-memory	18. The flash-storage ExpressCard of claim 16 wherein the serial control means comprises both a Universal-Serial-Bus (USB) controller, and a Peripheral Component Interconnect (PCI) Express controller; and wherein the connector means includes a differential pair of serial data lines that carry serial USB signals between the host and the controller means when using the USB controller, and a differential pair of PCI-Express-transmit serial data lines and a differential pair of PCI-Express-receive serial data lines that carry serial signals between the host and the controller means when using the PCI Express controller, whereby dual serial controllers allow communication with the host using either USB or PCI Express.

card; indicator means, connected to the input-output bus means, for indicating a status to a user in response to the dual-mode microcontroller means; activating-input means, connected to the input-output bus means, for receiving an input from the user, the activating-input means sending a user-activating signal to the dual-mode microcontroller means; main control program means, executed by the dual-mode microcontroller means, for detecting insertion of the removable flash-memory card, for detecting connection of the USB-memory key drive to the first connector means, and for detecting connection of the external USB host to the second connector means, for activating a USB peripheral mode when the external USB host is connected, but for activating a local-host mode when the external USB host is not connected, but the USB-memory key drive is connected, the main control program means causing the indicator means to display a mode status indicating the USB peripheral mode or the local-host mode; wherein the external USB host reads data from the removable flash-memory card through the dual-mode microcontroller means when operating in the USB peripheral mode; and flash-exchanger program means, executed by the dual-mode microcontroller means when operating in the local-host mode and the user-activating signal is received from the activating-input means, for blinking the indicator means and transferring data between the removable flash-memory card and the USB-memory key drive without an external USB host, whereby the flash-exchanger program means operates when the external USB host is not connected.	
19. The flash-card exchanger of claim 18 further comprising: second flash interface means, connected to the input-output bus means, for interfacing to a second type of removable flash-memory card.	19. An interleaved flash ExpressCard comprising: an ExpressCard connector for plugging into a host; a controller chip that has a microprocessor core, a program memory, a buffer memory, a serial controller, and a flash controller; a first flash-memory chip in a first channel; a second flash-memory chip in the first channel; a third flash-memory chip in the first channel; a fourth flash-memory chip in the first channel; a shared control bus having a write-enable signal, a read-enable signal, and latch-enable signals generated by the flash controller in the controller chip and driven to the first, second, third, and fourth flash-memory chips; a first data bus between the controller chip and the first and third flash-memory chip; a first shared ready signal generated by the first flash-memory chip and the second flash-memory chip and driven to the controller chip; a second data bus between the controller chip and the second and fourth flash-memory chip; and a second shared ready signal generated by the third flash-memory chip and the fourth flash-memory chip and driven to the controller chip; a first chip select generated by the controller chip and connected to the first and second flash-memory chip; a second chip select generated by the controller chip and connected to the third and fourth flash-memory chip; wherein the serial controller

	in the controller chip is a Universal-Serial-Bus (USB) controller that communicates to the host using a pair of differential USB data signals in the ExpressCard connector, or the serial controller in the controller chip is a Peripheral Component Interconnect (PCI) Express controller, a Firewire controller, a serial ATA controller, or a serial small-computer system interface (SCSI) controller; wherein access to the first and third flash-memory chips is interleaved; wherein access to the second and fourth flash-memory chips is interleaved.
20. The flash-card exchanger of claim 18 wherein the indicator means comprises: a first light-emitting diode (LED) that is lit when the removable flash-memory card is inserted into the first flash interface means; a second LED that is lit when the USB-memory key drive is connected to the first connector means and the external USB host is not connected to the second connector means; a third LED that is lit when the external USB host is connected to the second connector means; and a direction LED that is lit to indicate a direction of data transfer.	20. An interleaved dual-channel flash ExpressCard comprising: an ExpressCard connector for plugging into a host; a controller chip that has a microprocessor core, a program memory, a buffer memory, a serial controller, and a flash controller; a first flash-memory chip in a first channel; a second flash-memory chip in a second channel; a third flash-memory chip in the first channel; a fourth flash-memory chip in the second channel; a first shared control bus having a write-enable signal, a read-enable signal, and latch-enable signals generated by the flash controller in the controller chip and driven to the first and third flash-memory chips; a first data bus between the controller chip and the first and third flash-memory chip; a first ready signal generated by the first flash-memory chip and driven to the controller chip; a third ready signal generated by the third flash-memory chip and driven to the controller chip; a second shared control bus having a write-enable signal, a read-enable signal, and latch-enable signals generated by the flash controller in the controller chip and driven to the second and fourth flash-memory chips; a second data bus between the controller chip and the second and fourth flash-memory chip; and a second ready signal generated by the second flash-memory chip and driven to the controller chip; and a fourth ready signal generated by the fourth flash-memory chip and driven to the controller chip; wherein the serial controller in the controller chip is a Universal-Serial-Bus (USB) controller that communicates to the host using a pair of differential USB data signals in the ExpressCard connector, or the serial controller in the controller chip is a Peripheral Component Interconnect (PCI) Express controller, a Firewire controller, a serial ATA controller, or a serial small-computer system interface (SCSI) controller, wherein access to the first and third flash-memory chips is interleaved; wherein access to the second and fourth flash-memory chips is interleaved.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-2, 4 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sukegawa (US 5,812,814), and in view of Langan et al. (US 6,230,238).

As to claim 1, Sukegawa discloses **an ExpressCard** [figures 3, 9-10, 13-18; FIG. 9 is a block diagram of a single package LSI showing another embodiment of the present invention; FIG. 10 is a block diagram of the semiconductor memory system using the single package LSI shown in FIG. 9 (column 3, lines 25-30)]

comprising:

an ExpressCard connector for mating with a host ExpressCard connector on a host [the semiconductor memory system unit 420 has a card edge type connector 430 for connecting between the host system 1 and the host interface 320 in the semiconductor disk LSI 300 (column 11, lines 28-31)];

a first flash-memory chip for storing data [figure 1a-2 shows a plurality of flash EEPROM chips (101~112); figure 2; figure 10; figure 12; figure 16];

a second flash-memory chip for storing data [figure 1a-2 shows a plurality of flash EEPROM chips (101~112); figure 2; figure 10; figure 12; figure 16];

a controller chip [the host interface controller, figure 1a-1, 130] **coupled to the ExpressCard connector, for controlling communication to the host through the ExpressCard connector** [figure 1a-1];

a first flash-memory channel between the controller chip and the first flash-memory chip, the first flash-memory channel having a first data bus for communicating data between the controller chip and the first flash-memory chip [the corresponding first channel is DRIVE #0 of figure 2; a semiconductor memory system including a flash EEPROM comprises a first flash EEPROM included in the first memory drive, a second flash EEPROM included in the second memory drive, and means for controlling access to the first and second flash EEPROMs (abstract); in accordance with the present invention there is provided a peripheral semiconductor memory system including first and second memory drives. The system comprises a first flash EEPROM included in the first memory drive, a second flash EEPROM included in the second memory drive, and means for controlling access to the first and second flash EEPROMs (column 2, lines 17-24); see below];

a second flash-memory channel between the controller chip and the second flash-memory chip, the second flash-memory channel having a second data bus for communicating data between the controller chip and the second flash-memory chip [the corresponding second channel is DRIVE #1 of figure 2; a semiconductor memory system including a flash EEPROM comprises a first flash EEPROM included in the first memory drive, a second flash EEPROM included in the second memory drive, and means for controlling access to the first and second flash EEPROMs (abstract); in accordance with the present invention there is provided a peripheral semiconductor memory system including first and second memory drives. The system comprises a first flash EEPROM included in the first memory drive, a

second flash EEPROM included in the second memory drive, and means for controlling access to the first and second flash EEPROMs (column 2, lines 17-24); see below];

a shared control bus between the controller chip and the first and second flash-memory chips [figure 10 shows the shared READ/WRITE Control line; The flash EEPROM chips 101-106 and the IC slots 111 and 112 are connected to the controller unit 130 via a common read/write control line (R/W) (column 4, lines 23-26)];

a first response line from the first flash-memory chip to the controller chip for indicating completion of an operation by the first flash-memory chip [figure 1a-2 shows that each flash EEPROM chip has its own Ready/Busy (R/B) response line; each flash EEPROM chip 101-106 and each IC slot 111 and 112 is independently connected to the controller unit 130 via a chip select signal (each CS 1-8) line and a ready/busy signal (R/B) line (column 4, lines 26-29)]; **and**

a second response line from the second flash-memory chip to the controller chip for indicating completion of an operation by the second flash-memory chip [figure 1a-2 shows that each flash EEPROM chip has its own Ready/Busy (R/B) response line; each flash EEPROM chip 101-106 and each IC slot 111 and 112 is independently connected to the controller unit 130 via a chip select signal (each CS 1-8) line and a ready/busy signal (R/B) line (column 4, lines 26-29)],

whereby the ExpressCard has two channels [the corresponding first channel is DRIVE #0 of figure 2, and the corresponding second channel is DRIVE #1 of figure 2] **to th first and s cond flash-memory chips** [memory block 1 and memory block 2 of figure 2] **but a shared control bus to the first and second flash-memory chips**

[figure 10 shows the shared READ/WRITE Control line; The flash EEPROM chips 101-106 and the IC slots 111 and 112 are connected to the controller unit 130 via a common read/write control line (R/W) (column 4, lines 23-26)].

Regarding claim 1, Sukegawa does not explicitly show that **the first and the second channels have a first and second data bus**, respectively.

However, Langan et al. teach in their invention "Method and Apparatus for Accessing Misaligned Data from Memory in an Efficient Manner" a memory array where a first data bus and a second data bus are used to accommodate the high byte data and low byte data, respectively [figures 1 and 2].

The split of the high byte and low byte and their separate data bus provides an effective way of implementing a 16-bit wide stack in an 8-bit microcontroller environment whereby mis-aligned pushes and pops can be accomplished in a uniform and short same time period, the same as aligned push and pop operations [column 2, lines 17-21].

Therefore, it would have been obvious for one of ordinary skills in the art at the time of Applicants' invention to recognize the benefit of having a first data bus and a second data bus for the first and second channels, respectively, as demonstrated by Langan et al., and to incorporate it into the existing apparatus disclosed by Sukegawa to further enhance the capability of the memory device to support mis-aligned data transfer.

As to claim 2, Sukegawa teaches **the ExpressCard of claim 1 further comprising: a housing for enclosing the controller chip and the first and second**

flash-memory chips; wherein the housing has an opening on an insertion end for the ExpressCard connector [figures 3, 13, 15 and 17].

As to claim 4, Sukegawa teaches that the first response line carries a ready signal from the first flash-memory chip; wherein the second response line carries a ready signal from the second flash-memory chip, whereby separate ready signals are sent to the controller chip [figure 1a-2 shows that each flash EEPROM chip has its own Ready/Busy (R/B) response line; each flash EEPROM chip 101-106 and each IC slot 111 and 112 is independently connected to the controller unit 130 via a chip select signal (each CS 1-8) line and a ready/busy signal (R/B) line (column 4, lines 26-29)].

As to claim 16, refer to "As to claim 1" presented earlier in this Office Action.

7. Claims 3, 5-7, 9-15 and 17-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sukegawa (US 5,812,814), in view of Langan et al. (US 6,230,238), and further in view of Shaw ("Industry Transition from PC Card to ExpressCard Technology").

As to claim 3, neither Sukegawa nor Langan et al. teach that **the housing contains a cutout notch wherein a first width of the insertion end containing the ExpressCard connector is narrower than a second width of an opposite end that is opposite the insertion end**.

However, Shaw teaches in his paper "Industry Transition from PC Card to ExpressCard Technology" a number of the features of the ExpressCard standard, including that the housing contains a cutout notch wherein a first width of the insertion end containing the ExpressCard connector is narrower than a second width of an

opposite end that is opposite the insertion end [figure 5 shows the form factor of a 68-mm ExpressCard slot].

Since the limitation recited in this claim is part of the ExpressCard standard, it would have been obvious for one of ordinary skills in the art at the time of Applicants' invention to recognize the need to include this feature, as illustrated by Shaw, in order to meet the standard, hence lacking patentable significance.

As to claim 5, Sukegawa teaches that **the controller chip further comprises**: **a serial engine, coupled to the ExpressCard connector, for sending and receiving serial signals representing data and commands from the host** [figure 1a-1 shows the host interface for receiving commands from the host; figure 5 shows the flowchart of the communication between the controller and the host; see below]; **a flash-memory controller** [the access controller, figure 1a-2; the controller, figure 2, 130; access controller, figure 9, 332] **for generating control signals on the shared control bus to the first and second flash-memory chips** [figures 1a-2, 2 and 9]; **a central processing unit (CPU) for executing routines of instructions to transfer data between the serial engine and the flash-memory controller** [the CPU, figure 14, 611; figure 16; figure 18].

Regarding claim 5, neither Sukegawa nor Langan et al. teach **the use of a serial engine**.

However, Shaw teaches in his paper "Industry Transition from PC Card to ExpressCard Technology" a number of the features of the ExpressCard standard, including the support of the industrial standard USB (Universal Serial Bus) [page 1, first

and second paragraphs; figures 4 and 5 show the USB interface to a host chip set; the ExpressCard specification uses the PCI Express and the USB I/O interconnect standards of the PCISIG and USB-IF (page 2, first paragraph)].

Since the limitation recited in this claim is part of the ExpressCard standard, it would have been obvious for one of ordinary skills in the art at the time of Applicants' invention to recognize the need to include this feature, as illustrated by Shaw, in order to meet the standard, hence lacking patentable significance.

As to claim 6, Sukegawa teaches that **the controller chip further comprises an internal bus between the CPU, the serial engine, and the flash-memory controller** [figures 14, 16 and 18].

As to claim 7, Sukegawa teaches that **the controller chip further comprises**:

a system buffer [the data buffer, figure 1a-2, 133] **for temporarily storing data transferred between the serial engine and the flash-memory controller** [figure 1a-2; refer to "As to claim 5" for explanation of serial engine];

a scratch-pad random-access memory (RAM) for storing parameters used by the CPU [the DRAM, figure 1a-2, 133 and 150; DRAM, figure 9, 333; CPU, figure 14, 611];

and

a read-only memory (ROM) for storing the routines of instructions executed by the CPU [the main memory, figure 14, 612; figures 5-8 show the flowchart of the routines executed by the CPU].

As to claim 9, Sukegawa teaches that **the routines of instructions include**

routines to erase, read, or write data in the first or second flash-memory chips [figure 7, step 36 shows the operation of "copying data stored in the exchanged chip into the new chip"].

As to claim 10, Sukegawa teaches that **the controller chip further comprises**:

an input-output interface [I/O controller 1 and 2, figure 14, 613 and 614; I/O Interface, figure 10, 322] **for driving an indicator lamp when the flash-memory controller is reading or writing to the first or second flash-memory chips** [READ?WRITE control lines, figure 10]. Note that the use of indicator lamps for providing visual display of the status of equipment is a well-known and common practice in the art and lacks patentable significance.

As to claim 11, Sukegawa teaches that **the shared control bus comprises a read-enable signal and a write-enable signal that are connected to both the first and second flash-memory chips** [figure 10 shows the shared READ/WRITE Control line; The flash EEPROM chips 101-106 and the IC slots 111 and 112 are connected to the controller unit 130 via a common read/write control line (R/W) (column 4, lines 23-26)].

As to claim 12, Sukegawa teaches that **the shared control bus further comprises**:

a command latch enable signal to latch a command into the first or second flash-memory chips [COMMAND latch, figure 1a-1, 146];

an address latch enable signal to latch an address into the first or second flash-memory chips [Sector Number, figure 1a-1, 141; Cylinder, figure 1a-1, 144; Drive/Head, figure 1a-1, 145; Address Conversion Table, figure 1a-2, 150].

As to claim 13, Sukegawa teaches that **the shared control bus comprises a shared chip-select signal to enable the first flash-memory chip and the second flash-memory chip** [figure 1a-2, the chip select signals CS1~CS8; each flash EEPROM chip 101-106 and each IC slot 111 and 112 is independently connected to the controller unit 130 via a chip select signal (each CS 1-8) line].

As to claim 14, Sukegawa teaches that **the ExpressCard connector has a pair of differential data lines for communicating data and commands from the host to the controller chip** [figure 1a-1 shows the host interface for communicating data (143) and commands (146) from the host to the controller. Note that differential pair of data lines is well known in the art and is widely deployed in commercial electronic circuits to increase the rejection of common-mode noise, which leads to improved signal-to-noise ratio compared to single-ended data lines. See The Authoritative Dictionary of IEEE Standards Terms (IEEE Press, 7th edition, 2000, isbn 0-7381-2601-2; page 303: differential interconnect; page 304: differential signal).

As to claim 15, refer to "As to claim 5" presented earlier in this Office Action.

As to claim 17, refer to "As to claim 5" presented earlier in this Office Action.

Further, Shaw teaches in his paper "Industry Transition from PC Card to ExpressCard Technology" a number of the features of the ExpressCard standard, including the support of the industrial standard PCI express [page 1, first and second paragraphs; the

ExpressCard specification uses the PCI Express and the USB I/O interconnect standards of the PCISIG and USB-IF (page 2, first paragraph)].

Since the limitation recited in this claim is part of the ExpressCard standard, it would have been obvious for one of ordinary skills in the art at the time of Applicants' invention to recognize the need to include this feature, as illustrated by Shaw, in order to meet the standard, hence lacking patentable significance.

As to claim 18, refer to "As to claim 5" presented earlier in this Office Action. Further, Shaw teaches in his paper "Industry Transition from PC Card to ExpressCard Technology" a number of the features of the ExpressCard standard, including the support of the industrial standard PCI express [page 1, first and second paragraphs; the ExpressCard specification uses the PCI Express and the USB I/O interconnect standards of the PCISIG and USB-IF (page 2, first paragraph)].

Since the limitation recited in this claim is part of the ExpressCard standard, it would have been obvious for one of ordinary skills in the art at the time of Applicants' invention to recognize the need to include this feature, as illustrated by Shaw, in order to meet the standard, hence lacking patentable significance.

8. Claims 8 and 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sukegawa (US 5,812,814), in view of Langan et al. (US 6,230,238), in view of Shaw ("Industry Transition from PC Card to ExpressCard Technology"), and further in view of Piau et al. (US 6,859,856).

As to claim 8, neither Sukegawa nor Langan et al. teach **the use of an error-correction code (ECC)**.

However, ECC is well known in the art and is widely deployed in commercial electronic products for providing error detection and correction capability in order to improve data integrity and reliability. See Microsoft Computer Dictionary (Microsoft Press, 5th edition, 2002, isbn 0-7356-1495-4; page 196: error-correction coding; page 197: error detection and correction).

Further, Piau et al. teach in their invention "Method and System for a Compact Flash Memory Controller" a flash memory controller that is incorporated in a flash memory allowing the memory card to operate in either the PCMCIA mode or the IDE mode [abstract], where an ECC process [figure 1, 122] is included.

Therefore, it would have been obvious for one of ordinary skills in the art at the time of Applicants' invention to recognize that ECC is a well-known and commonly adopted technique, as illustrated by Piau et al., in order to meet the standard, hence lacking patentable significance.

As to claim 19, refer to "As to claim 1" and "As to claim 18" presented earlier in this Office Action. Further, Piau et al. teach the use of an ATA interface as part of the flash controller [figure 2, 203].

As to claim 20, refer to "As to claim 1" and "As to claim 18" presented earlier in this Office Action. Further, Piau et al. teach the use of an ATA interface as part of the flash controller [figure 2, 203].

9. ***Related Prior Art of Record***

The following list of prior art is considered to be pertinent to applicant's invention, but not relied upon for claim analysis conducted above.

- Inoue et al., (US 6,032,237), "Non-Volatile Memory, Memory Card and Information Processing Apparatus Using the Same and Method for Software Write Protect Control of Non-Volatile Memory."
- Dye, (US 6,145,069), "Parallel Decompression and Compression system and Method for Improving Storage Density and Access Speed for Non-Volatile Memory and Embedded Memory Devices."
- Liu et al., (US 6,567,373), "Small Silicon Disk Card with a USB Plug."
- Glad, (US 5,773,332), "Adaptable Communication Connectors."
- Lee et al., (US 6,854,984), "Slim USB Connector with Spring-Engaging Depressions, Stabilizing Dividers and Wider End Rails for Flash-Memory Drive."

Conclusion

10. Claims 1-20 are rejected as explained above.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sheng-Jen Tsai whose telephone number is 571-272-4244. The examiner can normally be reached on 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sheng-Jen Tsai
Examiner
Art Unit 2186

March 29, 2006

PIERRE BATAILLE
PRIMARY EXAMINER
5/31/06